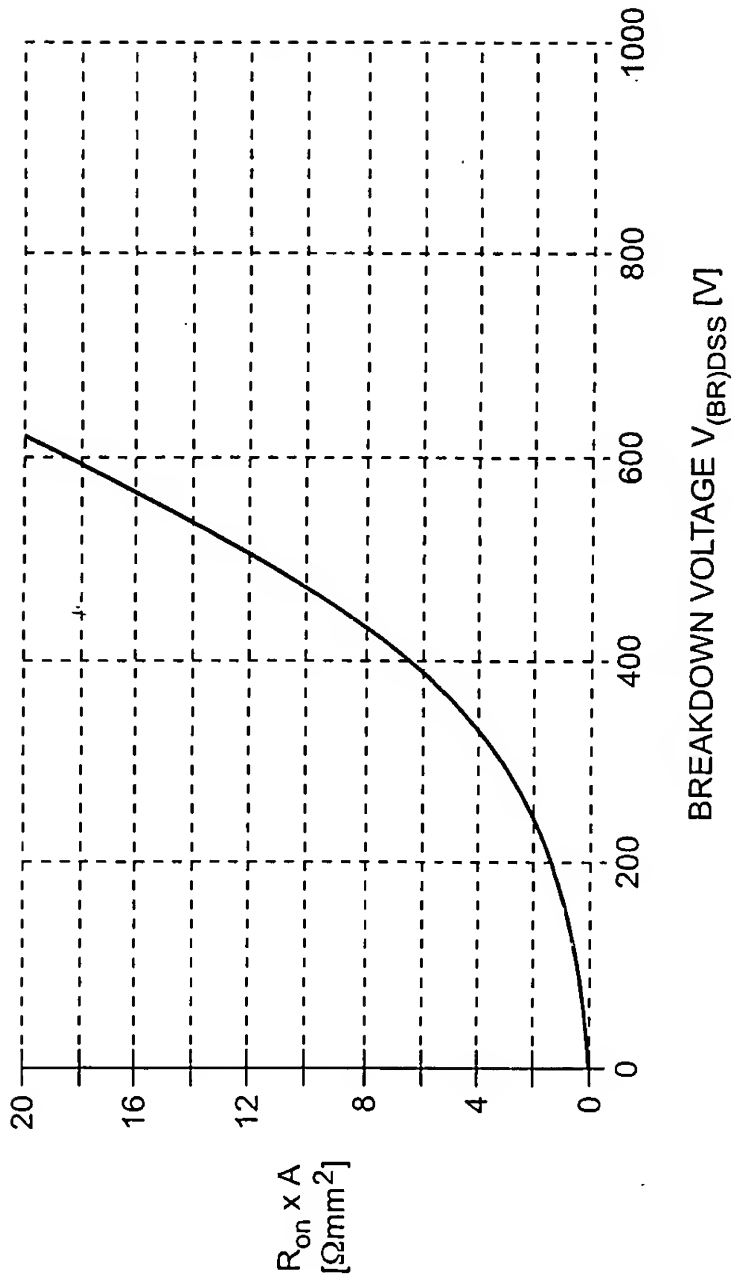


CONVENTIONAL MOSFET

FIG. 1

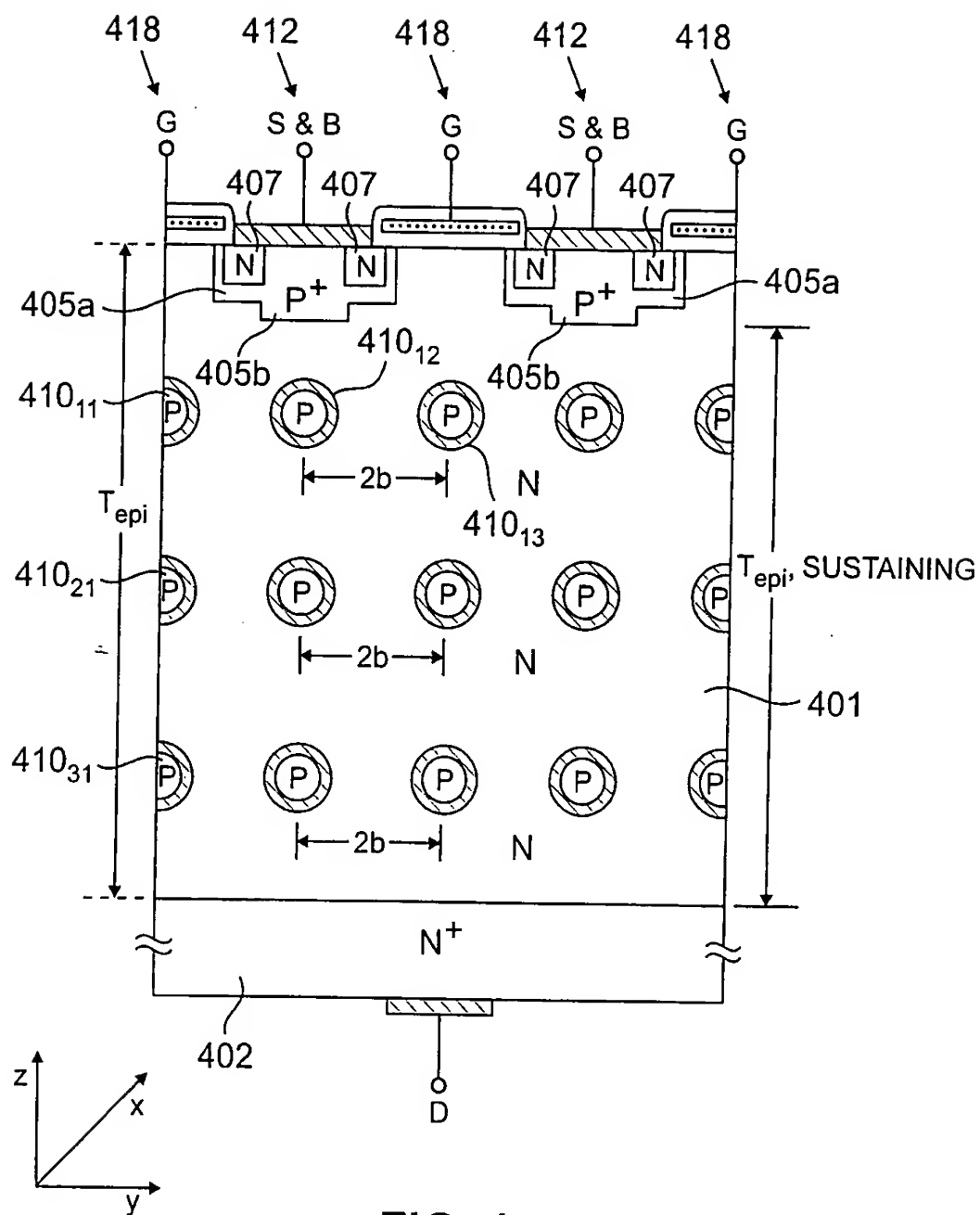
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THE SPECIFIC ON-RESISTANCE OF A VERTICAL DMOS TRANSISTOR WITH THE DOPANT DISTRIBUTION OF FIG. 1

FIG. 2

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STEP

1. EPITAXIAL DEPOSITION
2. FORM BARRIER LAYER
3. MASK AND ETCH BARRIER LAYER
4. ETCH THE TRENCH

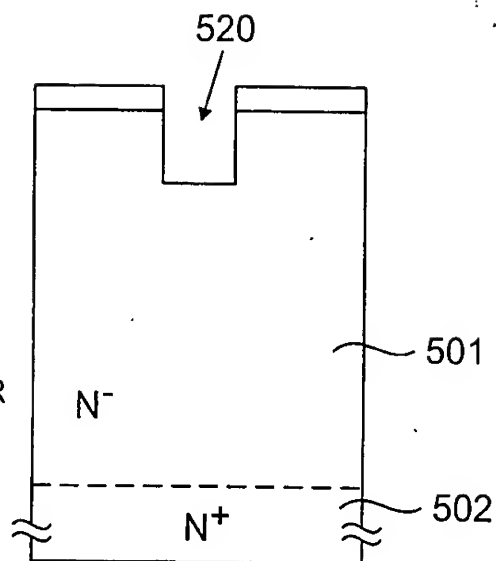


FIG. 5(a)

STEP

5. GROW AN OXIDE LAYER
6. IMPLANT DOPANT

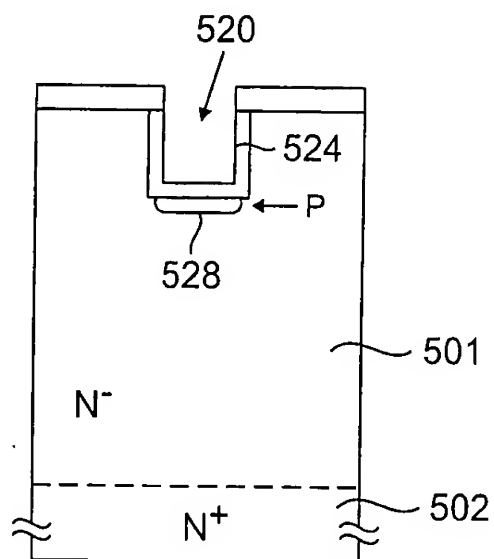
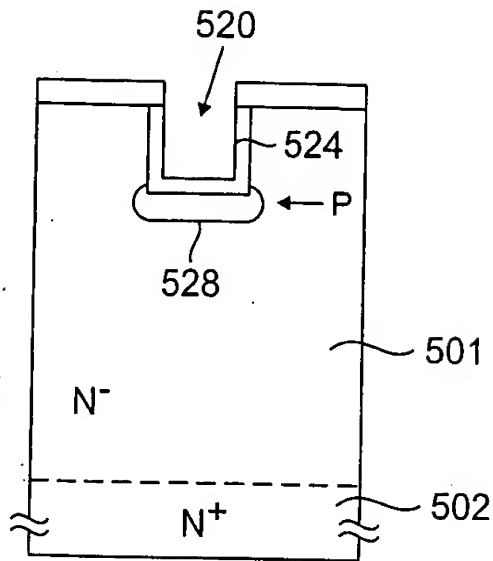


FIG. 5(b)

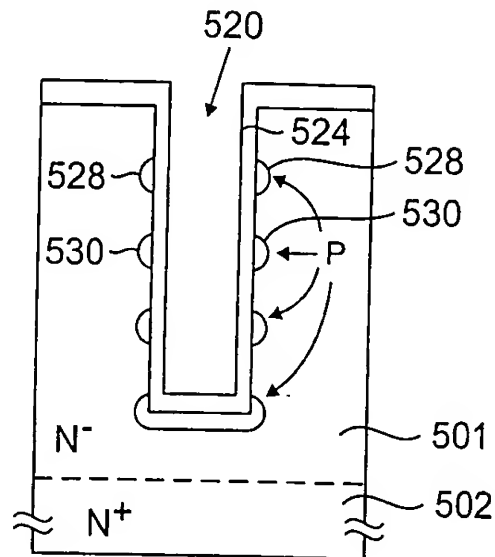
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STEP

7. HIGH TEMPERATURE DIFFUSION
8. ETCH OXIDE AT TRENCH BOTTOM

**FIG. 5(c)**STEP

9. REPEAT THE TRENCH ETCH STEP, THE OXIDE GROWTH STEP, THE DOPANT INTRODUCTION STEP, THE DRIVE-IN STEP, AND THE OXIDE ETCH STEP AS MANY TIMES AS REQUIRED
10. PERFORM THE OXIDE GROWTH STEP, THE DOPANT INTRODUCTION STEP, THE DRIVE-IN STEP, AND THE OXIDE ETCH STEP FOR THE LAST FLOATING ISLAND LAYER

**FIG. 5(d)**

STEP

11. REMOVE THE OXIDE FROM THE TRENCH BOTTOM TRENCH ETCH (THROUGH THE DIFFUSED P-TYPE LAYER)

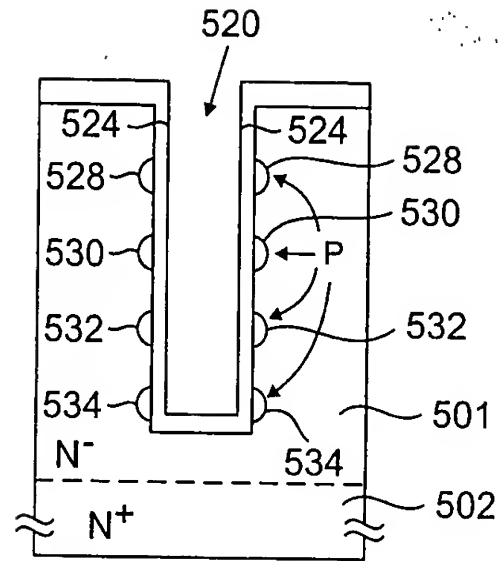


FIG. 5(e)

STEP

12. FILL THE TRENCH
13. PLANARIZE THE WAFER

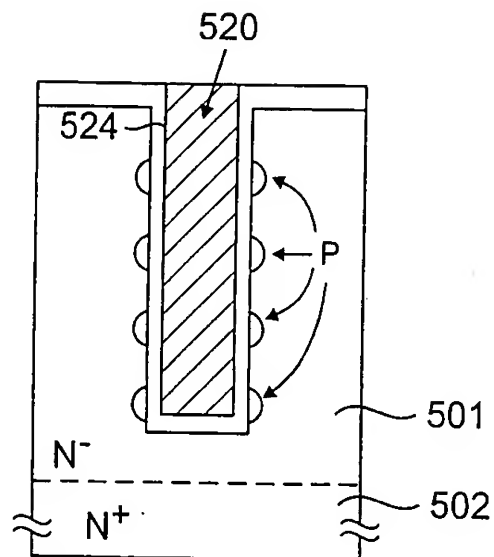


FIG. 5(f)